4.8 An 8Gb/s Transformer-Boosted Transmitter with >V_{DD} Swing

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Technology scaling along with decreasing supply voltage creates a tight tradeoff between high-speed and large-swing requirements in mixed-mode circuit design. One such example is a link transmitter where both large-swing and high-speed operations are desirable in order to deliver the high-frequency signal over a band-limited channel. The goal of this paper is to demonstrate a transmitter circuit that achieves high-frequency signaling with >V_{DD} voltage swings without stressing low-voltage transistors.

Typical transmitter pre-emphasis achieves an equalized channel response by attenuating low-frequency signal energy with the peak signal-swing limited by the supply voltage [1]. The proposed transformer-boosted transmitter emphasizes the high-frequency signal without reducing low-frequency energy by boosting above the supply rail. The concept is described in Fig. 4.8.1 as a single-ended design. In order to achieve the high-frequency signal boosting, a main current-mode driver, M_1, is enhanced with a boosting driver, M_2, that is driven through a transformer, L_1-L_2. Voltage coupling by the transformer is added to the output constructively by the appropriate direction of coupling, hence achieving larger high-frequency signal swing than the dc swing.

The design has several considerations for the choice of the inductances and resistances. First, the actual coupled voltage at the inductor L_1 can be expressed as ,

$$V_L = V_{C1} - V_{L1} = k\sqrt{L_1 L_2} \cdot dI_{SS2}/dt - L_1 \cdot dI_{L1}/dt$$

where V_{C1} and V_{L1} are the voltage from mutual coupling and the voltage drop by self inductance of L_1, respectively. The equation indicates that excessively increasing the inductance of L_1 has diminishing return. An optimal L_1 value exists that maximizes the coupled voltage. Increasing the inductance of L_2 results in greater boosting, but the voltage swing at node Y would exceed V_{DD}, hence, violating the voltage tolerance of the boosting driver, M_2. From the simulations, near-optimal L_1 and L_2 values are 0.6nH and 0.87nH, respectively. A second consideration is the choice of R_L. The coupled voltage V_L is divided by the load resistor, R_L and the 50Ω channel impedance. A smaller R_L is advantageous for more boosting. However, a smaller R_L causes lower dc swing (for a given drive current) and poor output matching. 32Ω is used as a compromise.

Figure 4.8.2(a) shows the differential design that is implemented on the test chip. In order to relieve the voltage stress on the boosting driver, a programmable resistor, R_{CM}, reduces the common-mode voltage at Z so that the peak signal at Y_1 and Y_{1B} can be controlled to be less than V_{DD}. Since the boosting by each driver is limited by the voltage tolerance of the devices, the total signal boosting can be doubled by using two transformers (TR_1 and TR_2) combined in series [2]. To help maintain the voltages within the tolerable values, the drain voltage is observed with a peak detector. Figure 4.8.2(b) illustrates the design. Ideally, the output settles at V_{peak}-V_t. The V_t variation from both the fabrication and the body effect is calibrated using an external input.

The source impedance of the transmitter is a consideration in the design as it may lead to secondary reflections and resonances on the transmission medium. The substantial capacitance from the ESD and the output pad limits the high-frequency matching even if the load resistanceR_L is 50Ω. Figure 4.8.3(a) illustrates the simulated S_{11} with an estimated capacitance for ESD, pad, and output device of 800fF. The inductance of the transformer in the signal path improves high-frequency matching by tuning out some capacitances as simulated in Fig. 4.8.3(b) with simple π-model inductor.

The transformer performance is critical to the design. A geometry that yields minimum parasitics while achieving sufficiently large coupling coefficient with the proper coupling direction, is targeted. Shown in Fig. 4.8.4, L_2 and L_{2B} in the boosting driver carry large currents, and thus are realized as a differential architecture in thick metal 8 with 15μm width. L_1 and L_{1B} in the main driver are two separate inductors and are laid out on the same layer. L_1 and L_{1B} are mutually coupled and the layout is such that their mutual coupling favors the signal boosting. The coupling coefficient obtained from ASITIC is 0.75 with L_1= 0.6nH and L_2=0.88nH. Two transformers are located 70μm apart to avoid coupling. A single N-port S-parameter model from the EM solver is used in time-domain simulations in Cadence.

Figure 4.8.5 shows the test-chip architecture. The chip consists of an 8Gb/s PRBS generator with 2^{31}-1 pattern, 5 stages of FO-3 CML buffers, the transformer-boosted transmitter, three 4b DACs that control the amount of boosting, and the peak detector. The 8Gb/s PRBS sequence is generated by multiplexing 2 phase-shifted 4Gb/s PRBS sequences [3]. The output can be switched to be either a random data or a 1010 pattern.

The prototype transmitter chip is fabricated in a 1.2V 0.13μm CMOS technology and occupies 1.8mm×1.7mm including pads and ESD. The die micrograph is shown in Fig. 4.8.7. The design is packaged in a 44-pin ceramic package. High-speed signals are injected and probed directly on-chip. Measured S_{11} from the output pad exhibits <-10dB for frequencies < 4GHz, as shown in Fig. 4.8.3. The difference from simulation is due to additional resistance from the supply/pad routing and probing. Figure 4.8.6(a) demonstrates the signal boosting of the transmitter operating at 8Gb/s. Operating at this mode, the I_{SS1} and I_{SS2}=I_{SS3} in Fig. 4.8.2 are 23mA and 57mA, respectively. With a 1.2V on-chip supply, the measured maximum high-frequency and dc swings are 1.42V_{pp} and 650mV_{pp}, respectively, thus achieving about 6.7dB of high-frequency boosting. Although simulation shows 2V_{pp} swing at 10Gb/s, shown in Fig 4.8.2(c), 1.42V_{pp} is the highest among this class. The boosting can be used for 1-tap of pre-emphasis and corresponds to a tap coefficient of α_1=0.37. The measured jitter is 25ps_{pp} at near end, where 14ps_{pp} is attributed to external clock noise. Peak detection is performed when transmitting a 1010 pattern to obtain the highest internal voltage. Measured peak detector output is 0.74V, which corresponds to 1.18V of peak value after calibration as shown in Fig. 4.8.6(b). The calibration measurement is done by externally injecting a sinusoid while varying the peak value. Fig. 4.8.6(c) is the far-end eye through the channel that has loss of 9dB at the Nyquist frequency.

References:

[1] P. Landman, et al., "A Transmit Architecture with 4-Tap Feedforward Equalization for 6.25/12.5Gb/s Serial Backplane Communications," *ISSCC Dig. Tech. Papers*, pp. 66-67, Feb., 2005.

[2] I. Aoki, et al., "Distributed Active Transformer – A New Power-Combining and Impedance-Transformation Technique," *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, pp. 316-331, Jan., 2002.

[3] F. Sinnesbichler, et al, "Generation of High-Speed Pseudorandom Sequences Using Multiplex-Techniques," *IEEE Trans. on Microwave Theory and Techniques*, vol. 44, pp. 2738-2742, Dec., 1996.

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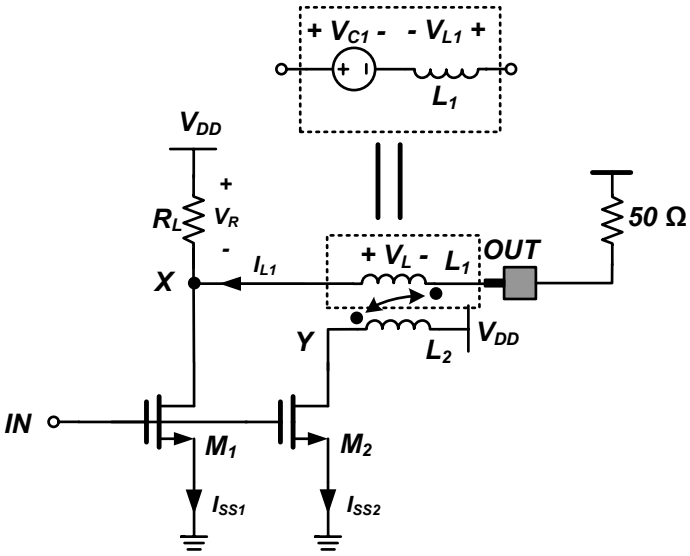

Figure 4.8.1: Concept of transformer-boosted transmitter.

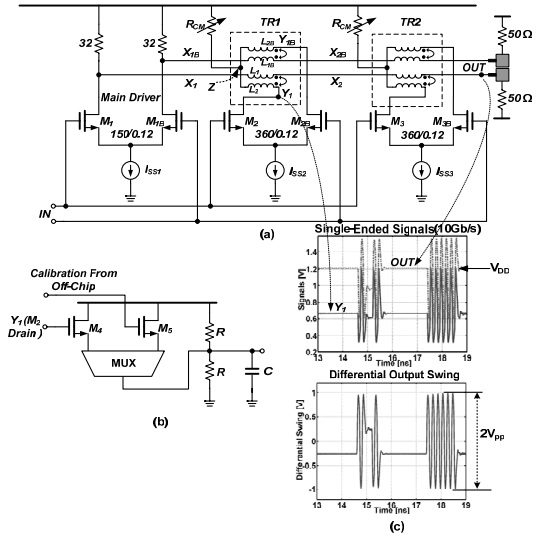

Figure 4.8.2: Circuit Implementation (a) Complete Transmitter (b) Peak Detector (c) Simulation.

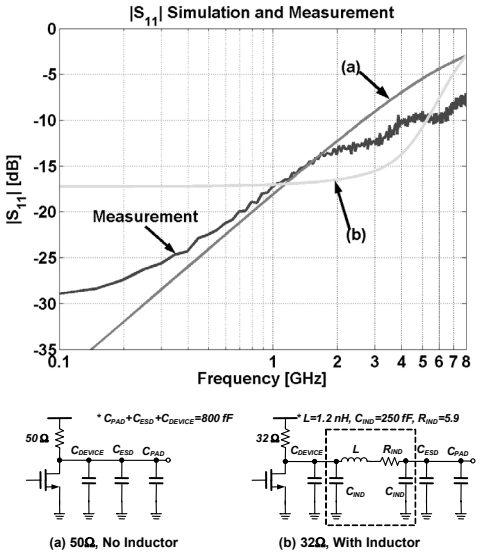

Figure 4.8.3: Simulated and measured S_{11}: (a) No inductor (b) With Inductor.

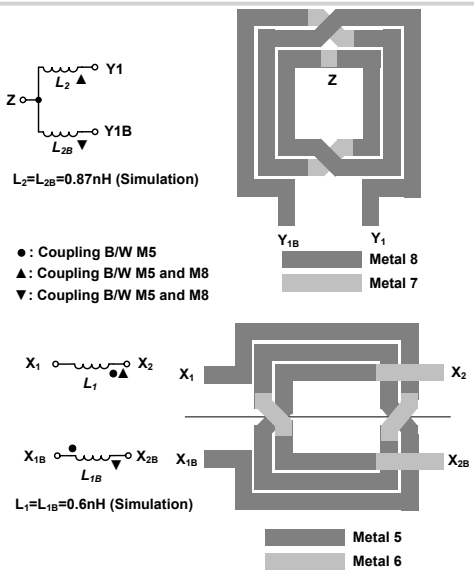

Figure 4.8.4: Transformer layout.

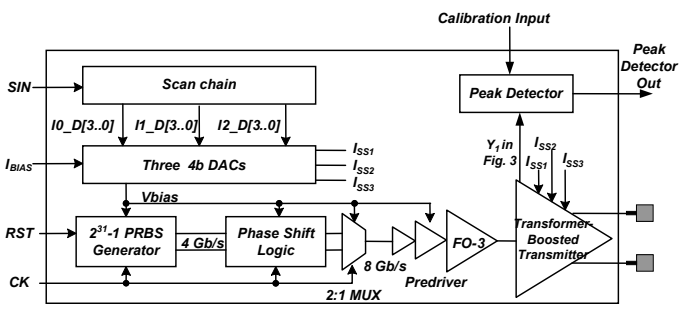

Figure 4.8.5: Prototype chip diagram.

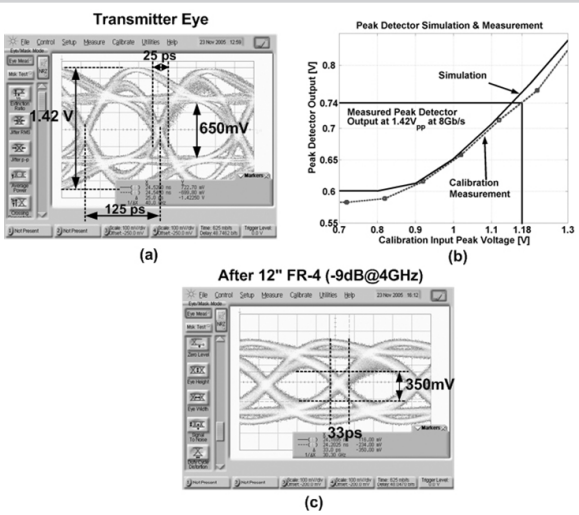

Figure 4.8.6: Measured performance: (a) Near-end eye (vertical scale: 200mV, horizontal scale: 31.25ps.) (b) Peak detector output (c) Eye after 9dB attenuation (vertical scale: 200mV, horizontal scale: 31.25ps.)

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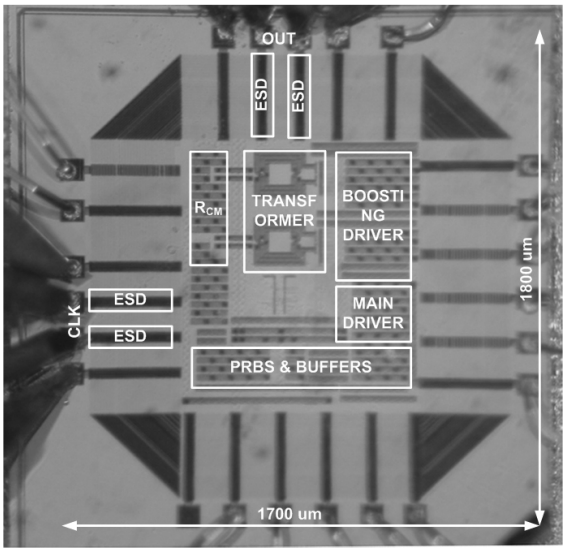

Figure 4.8.7: Chip micrograph.

